TRANSISTOR WITH REDUCED GATE-TO-SOURCE CAPACITANCE AND METHOD THEREFOR

FIELD OF THE INVENTION

The present invention relates generally to field effect transistors, and more particularly, to a field effect transistor with reduced gate-to-source capacitance.

BACKGROUND OF THE INVENTION

One type of high power transistor uses a plurality of polysilicon gate fingers located in an active area of a silicon substrate. A source and drain region are formed on each side of each of the gate fingers. A channel region is located directly below the gate fingers. The gate cross section for the shortest distance between source and drain is called gate length. The dimension perpendicular to this is the finger length or the transistor gate width. For a single transistor, multiple fingers might be connected in parallel to increase the gate width. The sum of all the finger lengths is then called the gate periphery. Assuming the cross sections of all fingers are identical, the power capability of a transistor is determined by the power capability of a unit finger length multiplied by the total periphery. The number of fingers that a high power transistor can have is determined by various limitations, including for example, the size of the package in which the high power transistor must fit. Also, increasing the length of the fingers increases the gate resistance (Rg) which is another important high frequency parameter. In one high power transistor, to overcome the increase in gate resistance, a low resistivity material, for example, a metal, is run parallel to the gate fingers over the source area to form a gate bus. The gate bus periodically contacts the gate fingers to reduce the gate resistance Rg. Gate pads are placed and sized to allow a contact from the gate

bus to be landed. However, lowering the gate resistance in this manner results in a higher parasitic gate-to-source capacitance (Cgs) because of the additional polysilicon gate area needed to facilitate the connection to the gate bus. The higher Cgs has an adverse effect on the performance of the transistor through an increase in the RC time constant and a change in the Cgs characteristic.

Therefore, there is a need to minimize the parasitic Cgs of the transistor while maintaining a low Rg.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates, in a top down view, a high power transistor in accordance with the present invention.

FIGs. 2 - 8 illustrate, in cross-sectional views along a line 8 - 8 of the transistor of FIG. 1, a method for forming the transistor of FIG. 1.

DETAILED DESCRIPTION

Generally, the present invention provides, in one embodiment, a high power transistor having a plurality of relatively long parallel gate fingers. Each of the gate fingers has a plurality of gate tabs for connecting the gate fingers to a metal gate bus. The gate fingers and plurality of gate tabs are over an active region. The metal gate bus is for reducing a resistance of the relatively long polysilicon gate fingers. To reduce a gate-to-source capacitance, a relatively thick local insulating layer is used between the gate tabs and the substrate. In the illustrated embodiment, the relatively thick insulator is about four times thicker than the gate dielectric layer that lies between the gate polysilicon and the channel region located directly underneath the gate polysilicon.

Reducing the gate-to-source capacitance allows the high power transistor to have higher frequency capability as compared to prior art transistors having the relatively thin gate oxide between the gate tab and the substrate.

FIG. 1 illustrates, in a top down view, a high power RF (radio frequency) transistor 10 in accordance with the present invention. Transistor 10 is a laterally diffused metal oxide semiconductor (LDMOS) transistor formed in a silicon substrate. In one embodiment, high power transistor 10 is a discrete device. In another embodiment, transistor 10 is implemented with other integrated circuits on a semiconductor die (not shown). Transistor 10 includes a plurality of parallel polysilicon gate fingers including gate fingers 12 and 14 formed over an active region in the silicon substrate. An active region is defined as being an area or region of the substrate that highly doped or otherwise has a low resistivity and is electrically part of one of the source, drain, or gate terminals of a transistor. The active region includes channel regions located below gate fingers 12 and 14 and the source and drain regions of the transistor 10 illustrated in FIG. 1. A heavily doped N+ drain region 22 is implanted within lightly doped drain region 20 as indicated by the parallel dashed lines in FIG. 1 that are between gate fingers 12 and 14. N+ source regions 19 and 25 are implanted on the sides of gate fingers 12 and 14 opposite from drain region 22. The amount of power the transistor can provide is determined by the number of gate fingers. There can be any number of gate fingers 12 and 14 and gate fingers 12 and 14 can be any length depending on the amount of available surface area on a semiconductor device having transistor 10. In effect, transistor 10 includes a plurality of transistors coupled in parallel.

Gate buses 56 and 58 are formed from a metal, or other relatively low resistivity material, on either side of gate fingers 12 and 14. The metal may be any metal used in semiconductor manufacturing including aluminum and copper. Gate buses 56 and 58 are connected together (not shown) to form one

gate connection. Gate tabs 32 and 36 are two of a plurality of gate tabs formed adjacent to gate bus 58 and are used to connect gate finger 12 to gate bus 58. Likewise, gate tabs 40 and 44 are two of a plurality of gate tabs used to connect gate finger 14 to gate bus 56. There can be any number of gate tabs for connecting a gate finger to a gate bus. All of the gates tabs are located within the active region that forms the source terminal of transistor 10. In other embodiments, the gate tabs may be located with the drain active region of a transistor. For purposes of illustration, only two gate tabs 32 and 36 are connected to gate finger 12 by tab connections 30 and 34, respectively. Gate bus 58 includes gate bus extensions 16 and 18 that extend from gate bus 58 to the gate tabs 32 and 36. The gate bus extension 16 is formed from gate bus 58 and extends over and is contacted to gate tab 32. The gate bus extension 18 is formed from gate bus 58 and extends over and is contacted to gate tab 32. Gate bus 56 includes gate bus extensions 26 and 28 for connecting to gate tabs 40 and 44, respectively. The size of gate tabs 32, 36, 40, and 44 depends, at least in part, on the size of the contact. Conventional semiconductor processing techniques are used to form the contacts.

In the past, the gate dielectric was formed over a relatively large area of the transistor and the gate tabs, being part of the gate polysilicon, were formed over the gate dielectric to insulate the gate tabs from the underlying substrate. The gate structure scales, or can be decreased in size, as semiconductor processes advance. However, the gate tabs cannot necessarily be scaled accordingly, and the effect of the parasitic capacitance associated with the gate tabs becomes more pronounced as the active gate structure is reduced in size. In accordance with one embodiment of the present invention, each of the gate tabs is formed over a relatively thick local oxide layer, or tab insulator. Gate tab 32 is formed over tab insulator 46, gate tab 36 is formed over tab insulator 48, gate tab 40 is formed over tab insulator 52, and gate tab 44 is formed over tab

insulator 54. In the illustrated embodiment, oxide layers 46, 48, 40, and 44 are about 100 nanometers (nm) thick and the gate dielectric under gate fingers 12 and 14 is about 240 angstroms thick. The use of a locally thick oxide layer reduces the parasitic capacitance associated with the gate tabs. In other embodiments the tab insulators may have a different thickness, that is, the tab insulators may be thicker than the gate dielectric to reduce capacitance. Also, in other embodiments, the locally thick oxide layer may be used under any other passive part of the gate polysilicon to reduce the parasitic capacitance. Note that the gate contacts are not shown in FIG. 1 but are shown in the cross sectional view of FIG. 8.

FIGs. 2 - 8 illustrate, in cross-sectional views along a line 8 - 8 of transistor 10 of FIG. 1, a method for forming high power transistor 10. FIG. 2 illustrates a semiconductor device having a P+ substrate 11 and an insulating layer 13. The insulating layer 13 is formed from an oxide grown on a surface of substrate 11 to a thickness of about 100 nm. Note that the conductivity type of the substrate may be different in other embodiments.

FIG. 3 illustrates a step of patterning insulating later 13 with a patterned photo resist 15 to form the gate tab insulators 46 and 52 of FIG. 1. Insulating layer 13 is etched to remove the oxide not covered by patterned photo resist 15.

FIG. 4 illustrates the semiconductor device after patterned photo resist 15 is removed to expose gate tab insulators 46 and 52. Gate tap insulators 46 and 52 are about 100 nanometers thick. In the illustrated embodiment, the gate tab insulators are about 4 times thicker than the gate dielectric.

FIG. 5 illustrates forming insulating layer 21 on the surface of substrate 11. Insulating layer 21 functions as a gate dielectric for the polysilicon gate fingers 12 and 14. In the illustrated embodiment, insulating layer 21 is about 240 angstroms thick. In other embodiments, insulating layer 21 may be a different thickness and may be formed from an oxide, nitride, or other insulating

material. Also, in other embodiments, insulating layer 21 may be either a low k or a high k dielectric.

FIG. 6 illustrates polysilicon gate tabs 32 and 40, tab connections 30 and 38, and gate fingers 12 and 14. The polysilicon is deposited over locally thick oxide layers 46 and 52 and insulating layer 21.

FIG. 7 illustrates the step of implanting N+ drain region 22 and lightly doped drain regions 20 and 24. The N+ source regions, as illustrated in FIG. 1, are also implanted at this step, but do not exist in the area directly under the gate polysilicon so are not visible in the cross-sectional views.

FIG. 8 illustrates metal contacts 17 and 23 formed on gate tabs 32 and 40. A metal drain contact 27 is formed over N+ drain region 22. Gate bus extensions 16 and 26 are formed over contacts 17 and 24. Source contacts are formed on the other side of substrate 11 (not shown). The source contacts are formed using conventional semiconductor processing techniques and are not important for the purpose of describing the present invention.

Locally thick oxide layers 46, 48, 40, and 44 reduce gate-to-source capacitance by reducing the capacitance of the gate tabs. Reducing the capacitance allows transistor 10 to have higher frequency capability and to be more linear as compared to prior art transistors having a relatively thin gate tab insulating layer.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all modifications of the invention which fall within the true scope of the invention.